REMARKS

The above preliminary amendments and following remarks are submitted in accordance with a Request for Continued Examination filed on even date and in response to the Final Official Action of the Examiner mailed on September 17, 2004. Having addressed all objections and grounds of rejection, claims 1-25, being all the pending claims, are now deemed in condition for allowance. Reconsideration to that end is respectfully requested.

The Examiner has prematurely made the pending official action final. It is premature, because he has presented a new grounds of rejection as to pending claims 1-10 and 21-25 with the application of newly cited prior art. In making the pending official action final, the Examiner states at paragraph 19:

> Applicant's amendment necessitated the new ground(s) of rejection presented in the Office action.

This statement is clearly erroneous and completely inconsistent with paragraph 2 which states:

> Claims 1-25 have been presented for examination in this application. In response to the last Office Action, no claims have been amended. No claims have been canceled or added.

Thus, the finality of the pending official action is clearly premature. As a result, Applicants respectfully request that this response be treated as an amendment of right.

Claims 11, 14, 16, and 19 have been rejected under 35 U.S.C. 102(b) as being anticipated by newly cited U.S. Patent No.

5,564,035, issued to Lai (hereinafter referred to as "Lai"). This ground of rejection is respectfully traversed as to the amended claimed as based upon clearly erroneous findings of fact.

Claim 11 is an independent method claim having four steps. These are:

> 1) Formulating a write memory request;
> 2) First checking for a level one cache memory hit in response to said write memory request;
> 3) Second checking for a level two cache memory hit in response to a hit found by said first checking step; and
> 4) Invalidating a portion of said level one cache memory corresponding to said write memory request in response to a hit found by said second checking step.

The claim has been amended to make it explicit that the first level cache memory is semi-store-in and the second level cache memory is both dedicated to the processor and is semi-inclusive. These limitations are fully supported in the specification and are summarized at page 6, line 19, through page 7, line 5. These environmental limitations are important to the efficiencies provided by the present invention.

The claims have been further amended to require checking for hits at the level one and level two cache memories. Such "checking" steps, particularly for the level two cache memory, is redundant in the system of Lai cited by the Examiner. This distinction is specifically admitted by the Examiner in his paragraph 4(a) which states in part:

> Because of the inclusion policy of the L2 cache 203, which dictates that all the contents of the L1 cache 202 are maintained in the L2 cache 203 (col.2, lines

35-57); the L2 cache 203 will also experience a cache memory hit in response to a hit in L1 cache 202.

As a result, the rejection of claim 11, and all claims depending therefrom is respectfully traversed.

Claim 14, as amended, depends from claim 11 and is limited by three additional steps including "recording location of data corresponding to said read memory request within said level one cache memory". In making his rejection, the Examiner cites column 6, line 45, through column 7, line 11, of Lai alleging the recording of the location of the data within the level two cache memory. In response thereto, claim 14 has been amended to require that the record of location of the data be made within the level one cache memory as fully supported in the specification. This is clearly not taught by Lai. The rejection of claim 14 is respectfully traversed.

In his rejection of claim 16, the Examiner again repeats the clearly erroneous finding of fact in citing Lai column 2, lines 52-57. This describes SNOOPing of a remote processor memory request rather than a cache first and second level cache memory misses of a local processor memory request. The rejection of claim 16, and all claims depending therefrom, is respectfully traversed.

In rejecting claim 19, the Examiner repeats the reasoning of his rejection of claim 14. However, claim 19 was already limited

to possessing the recording functionality within the level one cache. The rejection of claim 19 is respectfully traversed.

Claims 1-4 have been rejected under 35 U.S.C. 103(a) as being unpatentable over newly cited U.S. Patent No. 6,446,167, issued to Mayfield et al (hereinafter referred to as "Mayfield") in view of U.S. Patent No. 6,061,766, issued to Lynch et al (hereinafter referred to as "Lynch"), further in view of Lai. This ground of rejection is respectfully traversed for failure of the Examiner to present a *prima facie* case of obviousness as required by MPEP 2143.

Specifically, the Examiner admits at paragraph 8:

> However, Mayfield does not specifically teach a circuit for Snooping said system bus and a first logic which invalidates a corresponding level one cache memory location in response to either a non-local write as recited in the claim.

The reason that this is true of Mayfield is readily apparent from Fig. 1. The level two cache memory, L2 118, is shared by all of the processors within the system (i.e., processor 101 and processor 103). As a result, coherency of L2 is directly maintained without any SNOOP necessary or desirable. There is no purpose for circuitry to SNOOP Fabric 204.

As a result, the Examiner's statement regarding alleged motivation to modify Mayfield is legally inadequate and based upon clearly erroneous findings of fact. The Examiner states at paragraph 8:

> Since (sic) the technology for implementing a circuit for snooping a system bus was well known and since (sic) snooping a system bus provides a snoop process for ensuring cache coherency, an artisan would have been motivated to implement a circuit for snooping a system bus in the system of Mayfield.

In other words, the Examiner alleges it obvious to utilize a SNOOP circuit with Mayfield because it exists, even though superfluous. This cannot be reasonably asserted to be motivation to create the alleged combination, because it makes no sense. The rejection of claim 1, and all claims depending therefrom is respectfully traversed.

In rejecting claim 2, the Examiner states:

> As per claim 2, the combination of Mayfield and Lai does not specifically teach a second logic which inhibits said first logic from invalidating for mode 3 requests without ownership as recited in the claim.

Again, this is true because of the architectures of Mayfield and Lai. As explained above, Mayfield has no need to SNOOP the alleged system bus (i.e., Fabric 204) because it shares the level two cache memory (i.e., L2 118) with all processors within the system. As a result, "mode 3 with ownership" makes no sense, resulting in no motivation for the alleged combination. The rejection of claim 2 is respectfully traversed.

In rejecting claim 3, the Examiner admits:

> As per claim 3, the combination of Mayfield and Lai does not specifically teach third logic which invalidates said corresponding cache memory location in response to a SNOOP hit as recited in the claim.

As explained above, this is true, because of the architecture of the alleged combination. Again, there is no motivation for a SNOOP function; therefore, there is no motivation for additional SNOOP functionality. The rejection of claim 3 is respectfully traversed.

In rejecting claim 4, the Examiner again admits that Mayfield does not have the claimed limitations. However, even though this structure is superfluous, he concludes:

> Thus, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the system of Mayfield to include recording location of data in response to a level one cache read miss and a level two cache memory read miss because it was well known to maintain multiprocessor coherency as taught by Lai.

Not only is this statement clearly erroneous and nonsensical, it is incorrect as a matter of law. This is precisely the unsupported conclusion attacked by the Court of Appeals for the Federal Circuit stating in part:

> Broad conclusory statements regarding the teaching of multiple references, standing alone, are not "evidence". *In re Dembiczak*, 175 F.3d 994, 50 U.S.P.Q. 2d 1614 (Fed. Cir. 1999.

Therefore, the rejection of claims 4 is respectfully traversed for failure of the Examiner to make a *prima facie* case of obviousness by showing motivation in accordance with MPEP 2143.

Claim 5 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Mayfield, in view of Lynch, in view of Lai, and further in view of U.S. Patent No. 4,891,809, issued to Hazawa

(hereinafter referred to as "Hazawa"). This ground of rejection is respectfully traversed for failure of the Examiner to present a *prima facie* case of obviousness as required by MPEP 2143.

Claim 5, as amended, depends from claim 1 and is further limited by circuitry to invalidate a level one cache memory **location** in response to detection of a level two cache memory error. In addition to the lack of motivation and lack of reasonable likelihood of success issues addressed above, the alleged combination of four references does not contain all of the claim elements. Hazawa generates "pseudo-errors", but does not have anything to do with detecting real parity errors, as claimed. Perhaps more important, Hazawa has no circuitry to invalidate a particular cache memory **location**. Hazawa teaches no invalidation at all, but simply sets an error flag. This error flag has nothing to do with a particular location. The rejection of claim 5 is respectfully traversed.

Claim 6 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Mayfield in view of Lai. This ground of rejection as to amended claim 6 is respectfully traversed.

The Examiner admits:

> However, Mayfield does not specifically teach a first circuit to invalidate a corresponding portion of said level one cache memory in response to a level one cache memory write hit and a level two cache memory hit as recited in the claim.

Again, as explained above, this results from the architecture of Mayfield which utilizes a shared level two cache memory. However, to make the claimed invention more explicit, it has been amended to specifically require that the level two cache memory is dedicated to a single processor. This architecture is clearly not found in Mayfield. The rejection of claim 6 is respectfully traversed.

Claim 9 has apparently been rejected under 35 U.S.C. 103(a) as being unpatentable over Mayfield in view of Lai. This ground of rejection is respectfully traversed.

As with claim 14, claim 9 has been amended to require that the recording of the data location be made within the level one memory. This feature is not found within either Mayfield (as admitted by the Examiner) or Lai, as explained above. Therefore, the rejection of claim 9 is respectfully traversed.

Claims 7 and 8 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Mayfield, in view of Lai, and further in view of Lynch. This ground of rejection is respectfully traversed for failure of the Examiner to present a *prima facie* case of obviousness as required by MPEP 2143.

In alleging the combination supporting his rejection, the Examine states:

> Since (sic) the technology for implementing inhibiting a logic from invalidating mode 3 requests without ownership was well known and since (sic) inhibiting invalidating mode 3 requests without ownership **provides**

> **a snoop process** for ensuring cache coherency, an artisan would have been motivated to implement inhibiting invalidating mode 3 requests without ownership in the system of Mayfield and Lai. (Emphasis added)

Again, as explained above, Mayfield has no "SNOOP process", because it does not need one. A "SNOOP process" added to Mayfield is superfluous and thus cannot possibly be motivated in accordance with controlling law. As a result, the additional limitations found in claims 7 and 8 cannot be shown to be motivated. The rejection of claims 7 and 8 is respectfully traversed for failure of the Examiner to present a *prima facie* case of obviousness.

Claim 10 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Mayfield, in view of Lai, and further in view of Hazawa. This ground of rejection is respectfully traversed.

In addition to the issues raised above concerning the claim from which claim 10 depends, the alleged combination does not have circuitry which invalidates a "corresponding portion" of the level one cache memory. In fact, the Examiner does not even consider the claimed elements. Instead, he states:

> Hazawa discloses invalidating a level one cache memory in response to a level two cache memory generating a parity error (col. 3, lines 38-48).

This finding is clearly erroneous, because shows only generation of a "pseudo-error" by Diagnostic Unit 1. There is no parity error generated by Cache Memory Unit 2. The Examiner's statement

is also legally irrelevant, because it does not address the claimed invention. The rejection of claim 10 is respectfully traversed.

Claims 12-13 and 17-18 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Lai in view of Lynch. This ground of rejection is respectfully traversed for the reasons discussed below.

Each of these claims depend from either amended claim 11 or amended claim 16 which are deemed patentable over the alleged rejection as anticipated by Lai for the reasons presented above. The embodiment of Lai relied upon by the Examiner for his rejection of claims 11 and 16 is the fully inclusive prior art example shown at Fig. 3 of Lai. One would not combine that embodiment with Lynch to add the claimed limitations of claims 12-13 and 17-18 because such additions would be superfluous. Lai has no mode 3 with ownership, because this would make no sense in the applied architecture of Lai which employs full inclusion of level one cache memory in level two cache memory. The Examiner continues to mix architectures in ways which do not make any sense. Similarly, Lai has no need for the claimed elements of claims 13 and 18. The fully inclusive architecture chosen by the Examiner does not and cannot utilize these elements. The rejection of claims 12-13 and 17-18 is respectfully traversed.

Claims 15 and 20 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Lai in view of Hazawa. This ground of rejection is respectfully traversed for the reasons provided below.

Both claims 15 and 20 require detection of a parity error. Hazawa only shows generation of a "pseudo-error". There is no disclosure of an actual parity error or structure in response thereto. Furthermore, claim 15 requires invalidation of a "portion" of the data, whereas claim 20 requires invalidation of an "element". Hazawa does not invalidate any particular portion or element. It simply sets a flag with regard to the entire cache memory. The rejection of claims 15 and 20 is respectfully traversed.

Claim 21 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Mayfield in view of Hazawa. This ground of rejection is respectfully traversed.

Claim 21 requires "a data element having a parity error stored in said level two cache memory" and "a facility which detects said parity error of said data element and invalidates a corresponding data element within said level two cache memory". The alleged combination does not have these elements. Perhaps acknowledging this lack of teaching, the Examiner states:

> Hazawa discloses invalidating data in a level two cache memory in response to a parity error of a data element to provide a cache memory with an error checking mode [col. 3, lines 38-51; col. 3, lines 38-59].

This statement ignores both the clear language of Applicants' claims and the clear teaching of Hazawa. Hazawa shows no "data element having a parity error" and no invalidation of a "corresponding data element". The rejection of claim 21 is respectfully traversed.

Claim 22 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Mayfield, view of Hazawa, and further in view of Lynch. This ground of rejection is respectfully traversed.

In addition to the issues raised with regard to claim 21 from which claim 22 depends, the Mayfield and Lynch systems are incompatible. Therefore, the rejection of claim 22 is respectfully traversed.

Claims 23-25 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Mayfield, in view of Hazawa, in view of Lynch, and further in view of Lai. This ground of rejection is respectfully traversed because the Examiner has again alleged the combination of incompatible architectures for the purpose of adding superfluous functionality as explained in detail above. The rejection of claims 23-25 is respectfully traversed.

Having thus responded to each objection and ground of rejection, Applicants respectfully request entry of this amendment and allowance of claims 1-25, being the only pending claims.

Please charge any deficiencies or credit any overpayment to Deposit Account No. 14-0620.

Respectfully submitted,

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By his attorney,

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